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ECe 3200-01 Lab 2

Four Resistor Biasing of MOSFET and JFET in the Active Region

**Objective:**

The objective of this lab is to measure the biasing stability of the N-channel MOSFET and JFET transistor circuits and will validate the results by calculation and simulation. The learning outcome will be a foundation for the design of small signal amplifiers later in the course.

**Procedure:**

1. Set up the MOSFET and the JFET transistor circuits, one at a time, according to the diagram shown in fig.1.
2. Adjust the power supply to Vcc = 22 V. If the power supply has a current limiter set it to 100 mA as a measure of safety.
3. Measure IDq and VDSq of both circuits each time as the transistors are changed
4. Determine the % of variation in the bias quantities due to changing of the transistor.

# **Schematics and Results:**

# Diagram, schematic Description automatically generated

A screenshot of a computer

Description automatically generated with medium confidence

**MEASUREMENT 1**

Build the circuit with **standard resistor** values and measure the drain currents IDq and drain-to-source quiescent voltage (VDSq) in both circuits:

IDq (meas.) = 1.7844 mA VDSq (meas.) = 11.89 V **MOSFET**

IDq (meas.) = 1.4652 mA VDSq (meas.) = 11.11 V **JFET**

**MEASUREMENT 2 (DATA from Lecture)**

Now replace both transistors with another random one from the same batch and repeat the step. Record the new results:

IDq (meas.) = 1.651 mA VDSq (meas.) = 10.6 V **MOSFET**

IDq (meas. ) = 2.21 mA VDSq (meas.) = 8.64 V **JFET**

What is the % of variation in the Q-point as the transistors were replaced?

IDq (% change) = 7.68285%, VDSq (% change) = 10.85% MOFSET

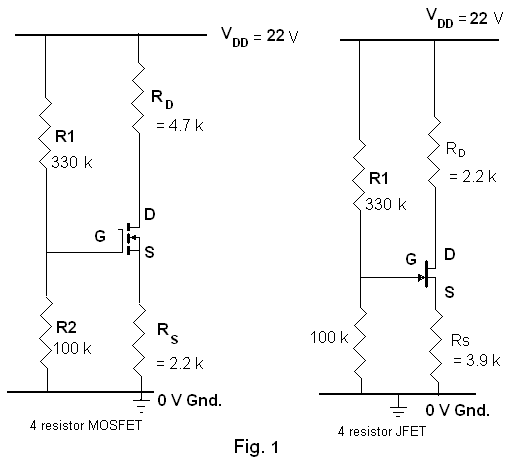
IDq (% change) = 50.832%, VDSq (% change) = 22.23% JFET

**DATA FROM INSTRUCTOR:**

**MOSFET**: For the 1st (ref.) MOSFET take VTN = 1.5 V and KN ≈ 300 mA/ V2.

**JFET**: For the 1st (ref.) JFET take IDSS = 6.2 mA and VP = - 2.5 V.

Both transistors were tested at a constant voltage of, VDS ≈ 12. V.



**Calculations:**

(MOSFET)

(JFET)

**Analysis**

IDq (% change) = 7.68285%, VDSq (% change)= 10.85% MOFSET

IDq (% change) = 50.832%, VDSq (% change) = 22.23% JFET

**Conclusion:**

As a result of this lab, I was able to familiarize myself with making measurements on the biasing stability of a MOSFET and JFET transistor circuits. Although I was not able perform the lab physically, I was still able to visualize the circuit with the help of Pspice, and the zoom meeting provided. Based off the lab from last week, I thought this lab was straightforward and informative as MOSFETs and JFETs are one of the foundational transistors used for small signal amplifiers.

**Analysis & Results:**

1. **Calculations:**

**MEASUREMENT 1**

(NPN)

= 1.440 mA

= 6.315 V

(PNP)

1.4242 mA

= 6.42 V

**MEASUREMENT 2**

(NPN)

= 1.440 mA

= 6.315 V

(PNP)

1.4242 mA

= 6.42 V

1. **Simulation:**

Diagram, schematic

Description automatically generated

*Figure 2: Voltage measurements using 2N2222 and 2N3906 transistor with*

Graphical user interface

Description automatically generated

*Figure 3: Current measurements using 2N2222 and 2N3906 transistor with*

Diagram, schematic

Description automatically generated

*Figure 4: Voltage measurements using 2N2222 and 2N3906 transistor with*

**Conclusion:**

This lab was conducted to examine the differences in biasing of an NPN and PNP. As a result of this lab, I was able to better understand making measurements on the biasing stability of an NPN and PNP transistor circuits, as well as how the biasing of these transistors produce certain current values. Although I was not able perform the lab physically, I was still able to visualize the circuit with the help of pSpice, and the zoom meeting provided. Having pSpice also allowed me to adjust the β value for each transistor and, from there, compare the percent variation between the quiescent values across the NPN and PNP. I thought this lab was relatively simple yet informative as it will become a foundation for small signal amplifiers for future labs from here on out.